## REMARKS

The application has been carefully reviewed in light of the Office Action dated April 7, 2004. Claims 18, 20, 31 and 34 have been amended. Claims 18-37 remain pending in this case.

Claims 26-33 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicants respectfully traverse the rejection and request reconsideration. The limitations "DC signal" and "DC input waveform" recited in claims 26, 27, 31 and 32 are disclosed at least at FIG. 3 of the application which depicts a portion of the clock signal 260 as being alternating high and low and another portion of the clock signal 260 being non-alternating, or DC. FIG. 3 also depicts a portion of the DLL output signal as being alternating and another portion 270 as being non-alternating, or DC. FIG. 3 is also described in the specification at pages 10 and 11. Applicants respectfully submit that such disclosures do teach the above-recited limitations to a person of ordinary skill in the art; and, therefore, the rejection should be withdrawn.

Claims 18-25 and 31-33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Shinozaki (U.S. Patent No. 5,990,730). Applicants respectfully traverse the rejection and request reconsideration.

Claim 18 recites a method of forming a memory integrated circuit comprising coupling a first clock input of a switching device to a clock input terminal and "coupling a second control input of [the] switching device to [a] mode-control input terminal, <u>said mode-control input terminal being adapted to receive a power-up/power-down signal signifying a power-up/power-down mode of said memory integrated circuit</u>." [Emphasis added.]

Shinozaki, to the contrary, fails to teach or suggest that a mode-control input terminal is adapted to receive a power-up/power-down signal signifying power-up/power-down mode of the semiconductor memory device 10. Rather, the Lockz signal being

received by the stop circuit 49 signifies when the DLL circuit 22 should start and stop adjusting timings of the variable delay circuit 43. Shinozaki at FIG. 5, column 9, lines 3-10. That is, the Lockz control signal signifies when the semiconductor device 10 operates in a normal mode rather than a mode in which the variable delay timing is adjusted. This is very different from a control signal signifying power-up/power-down of the semiconductor device 10, which is in no way taught or suggested by Shiozaki.

Claim 31 recites a clock signal received at an output of a delay line, said clock signal comprising a first signal portion having a periodic signal characteristic present during a first time interval signifying a power-up mode of a memory integrated circuit including said delay line and when a periodic input waveform is received at an input of said delay line. Claim 31 also recites that the clock signal also comprises "a second signal portion having a DC signal characteristic . . . present during a second time interval signifying a power-down mode of said memory integrated circuit and when a DC input waveform is received at said input of said delay line." [Emphasis added.]

Claim 31 is allowable over Shinozaki at least for the same reasons mentioned above in connection with claim 18 and also because Shinozaki fails to teach or suggest a second signal portion having a DC signal characteristic present during the second time interval signifying a power-down mode of the memory integrated circuit and when a DC input waveform is received at the input of the delay line, as defined by claim 31.

Claim 20 recites a method of operating a memory integrated circuit comprising "switchingly controlling an application of a periodic clock signal to an input node of a delay line . . . whereby during a first time interval, in which said memory integrated circuit is in a power-up mode, an output signal of said delay locked loop alternates and during a second time interval, in which said memory integrated circuit is in a power-down mode, said output signal of said delay locked loop does not alternate." [Emphasis added.]

At least for the same reasons mentioned above in connection with claims 18 and 31, claim 20 is also allowable over Shinozaki.

Claims 19, 21-25, 32 and 33 depend from claims 18, 20 and 31 and are also allowable at least for the reasons mentioned above and also because Shinozaki fails to teach or suggest the respective inventive combinations defined by claims 19, 21-25, 32 and 33.

Claims 26-30 and 34-37 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Applicants' admitted prior art (AAPA). Applicants respectfully traverse the rejection and request reconsideration.

Claim 26 recites a method of operating a memory integrated circuit comprising "receiving a DC signal at [an] input of [a] delay locked loop delay line." AAPA, to the contrary, discloses an external clock 74 coupled to the input of the delay locked loop 80. See Application at FIG. 1. The clock signal received by the DLL is alternating, which is precisely the cause of the problem being solved by the invention. The introduction of a DC signal at the input of the DLL eliminates the alternating of the individual delay elements within the DLL, thereby reducing power consumption of the memory integrated circuit. At least for these reasons, claim 26 is allowable over AAPA.

Claim 34 recites a memory integrated circuit device comprising "controlling means for controlling an externally generated periodic clock signal depending upon whether said memory integrated circuit device is in a power-up mode or a power-down mode, said controlling means coupled to [an] input of [a] delay line." [Emphasis added.] AAPA fails to teach or suggest controlling the externally generated periodic clock signal based on a power-up/power-down mode of the memory integrated circuit device. At least for these reasons, claim 34 is allowable over AAPA.

Claims 27-30 and 35-37 depend from claims 26 and 34 and are allowable at least for the same reasons mentioned above and also because neither AAPA nor any other of the cited references teaches or suggests the respective inventive combinations defined by claims 27-30 and 35-37.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection and to pass this application to issue.

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Respectfully submitted,

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